# Matthew Hartensveld, PhD

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## **Summary**

Seasoned semiconductor expert with a robust track record in the industry. Proficient in semiconductor fabrication, device physics, and advanced microsystems. Demonstrated leadership in both corporate and academic settings, with significant contributions to the field evident by 18 scientific publications.

## **Key Skills**

Technical Expertise	Simulations & Modeling
Micro-LEDs	Device Physics Simulations
Transistors	TCAD
Gallium Nitride Material Fabrication	Electrical Modeling
Crystal Growth	SPICE Modeling
Failure Analysis	Mask Layout
Comprehensive fabrication expertise	FDTD Simulations

## **Experience**

## CTO & CO-FOUNDER | INNOVATION SEMICONDUCTOR | SEPTEMBER 2019 - PRESENT

- Technical Leadership: Spearheaded all technical aspects, from device physics simulations, mask design, to device testing, ensuring the company remained at the forefront of industry innovations.
- · Innovation: Pioneered novel monolithic LED-FET technology and color tunable InGaN LEDs compatible with existing semiconductor infrastructure.
- Patent Development: Authored and prosecuted five patents, showcasing the company's pioneering work in the semiconductor space. (Refer to the patent section for details.)
- Business Acumen: Delivered compelling business presentations to stakeholders, securing buy-in for strategic initiatives and fostering partnerships.
- · Production Oversight: Collaborated closely with the production foundry, ensuring alignment with company objectives and addressing production challenges.
- Team & External Management: Supervised external contract engineers, ensuring timely and quality delivery of projects.
- · Startup Challenges: Navigated the challenges and complexities of a startup environment.

#### RESEARCH ASSISTANT | ROCHESTER INSTITUTE OF TECHNOLOGY | MAY 2018 - MAY 2021

- · Invented vertical nanowire GaN transistors.
- Developed GaN LEDs for alternative current operation.
- · Conducted research on various surface treatments for GaN.
- · Investigated the integration of GaN and Si, as well as flexible nanowires.
- Examined AlGaN deep ultraviolet nanowires with reverse taper.
- · Created unique GaN processes exclusive to the lab.
- · Advanced ideas from simulation to fabrication to characterization.

## INTERN | TEXAS INSTRUMENTS | MAY 2017 - AUG 2017

- · Collaborated with a team on a BiCMOS process.
- · Optimized an RTP Spike anneal step.
- · Ran statistical analysis of sheet resistances.

#### INTERN | NORTHROP GRUMMAN ADVANCED TECHNOLOGY LAB | MAY 2016 - AUG 2016

- · Implemented a new silicide process for SiC SITs, resulting in improved performance.
- · Innovated a bi-layer resist lift-off process for improved fabrication efficiency.
- · Determined the metal work function in the SiC process through testing and analysis.

## INTERN | NORTHROP GRUMMAN ADVANCED TECHNOLOGY LAB | JUNE 2015 - DEC 2015

- · Created a metal lift-off for GaN devices.
- · Conducted a DOE to optimize a Bosch process.
- · Modeled capacitor lifetimes for time to failure.

## **Education**

#### DOCTOR OF PHILOSOPHY, MICROSYSTEMS ENGINEERING | 2021 | RIT

Dissertation: Advanced Nanostructured III-Nitride LEDs for Display Applications scholarworks.rit.edu/theses/10779

#### MASTER OF SCIENCE, MATERIAL SCIENCE & ENGINEERING | 2018 | RIT

Thesis: Optimization of Dry and Wet GaN Etching to Form High Aspect Ratio Nanowires scholarworks.rit.edu/theses/9835

#### BACHELOR OF SCIENCE, MICROELECTRONIC ENGINEERING | 2018 | RIT

Capstone Project: Design of a 30 nm gate length vertical GaN nanowire transistor doi.org/10.1109/LED.2018.2886246

#### **Patents**

- [1] M. Hartensveld and J. Zhang "Nanowire Light Emitting Switch Devices and Methods Thereof," 11011571, 2021. Patent regarding vertically integrated LED-FET.
- [2] M. Hartensveld and J. Zhang "Capacitive Control of Electrostatic Field Effect Optoelectronic Device," 2019, Patent pending. Capacitive integrated control over charges in optoelectronic devices.
- [3] M. Hartensveld "Monolithic Semiconductor LED Display Systems and Methods Thereof", 2020,
- Patent pending. Integrated transistor logic in a micro-LED display system.

  [4] M. Hartensveld "Volume Engineering for LEDs and Methods Thereof" 2021. Patent pending.
- [4] M. Hartensveld "Volume Engineering for LEDs and Methods Thereof", 2021, Patent pending. Engineering the volume of the n-type and p-type regions for reduced LED efficiency droop.
- [5] M. Hartensveld "Monolithic Color-Tunable Light Emitting Diodes and Methods Thereof", 2022, Patent pending. InGaN color tunable LEDs engineered with differing crystal planes and strain reduction.
- [6] M. Hartensveld "Color-Tunable LED Elements and Display Systems and Methods Thereof", 2023, Patent Pending. InGaN color tunable LEDs growth method and further integration methodology.
- [7] M. Hartensveld "**Optoelectronic Isolations and methods thereof**", 2023, Patent Pending. Novel monolithic isolation structure for flexible circuit design and high-resolution passive matrixes.

#### Select Publications

[1] M. Hartensveld and J. Zhang "Monolithic Integration of GaN Nanowire Light-Emitting Diode with Field Effect Transistor," *IEEE* EDL, vol. 40, no. 3, p. 427-430, 2019, doi: 10.1109/LED.2019.2895846.

- [2] M. Hartensveld, G. Ouin, C. Liu, and J. Zhang "Effect of KOH passivation for top-down fabricated InGaN nanowire light emitting diodes," *J. Appl. Phys.*, vol. 126, no. 183102, 2019, doi: 10.1063/1.5123171.
- [3] M. Hartensveld "**Proposal and realization of V-groove color tunable µLEDs**", *Optics Expr.*, vol. 30, no. 15, p. 27314-27321, 2022, doi: 10.1364/0E.462177.
- [4] M. Hartensveld "**Proposal and realization of vertical GaN nanowire static induction transistor**", *IEEE EDL*, vol. 40, no. 2, p.259-262, 2018, doi: 10.1109/LED.2018.2886246.

More available at: scholar.google.com/citations?hl=en&user=AwPsN0oAAAAJ&view\_op=list\_works

#### **Awards**

#### **SEMICON 20 UNDER 30 | SEMI | 2023**

SEMICON West's 20 Under 30 is a distinguished awards program that identifies the industry's brightest young leaders who demonstrate outstanding leadership, practice productive collaboration, and have demonstrated success in their careers in microelectronics.

## **EMERGING LEADER AWARD | RIT | 2023**

This award is presented to KGCOE alumni who graduated within the last ten years, and it recognizes your professional accomplishments as well as, your dedication, support, and service to the college and RIT.

#### RENAN TURKMAN SCHOLAR AWARD | RIT | 2018

Demonstrated excellence in the field of microelectronics.

## **OUTSTANDING PERFORMANCE | NORTHROP GRUMMAN | 2015**

Helped the ATL Argon team overcome obstacles and challenges to meet the program's timetable for delivery.

# **Personal Projects**

#### HOME CLEANROOM

Fabricating homebrew transistors and devices since high school. The lab is complete with custom built/heavily modified tools including: sputtering/etch system, sub-micron lithography system, spin-coater, particle counter, tube furnace, semiconductor parameter analyzer, and probe station.

#### REVERSE ENGINEERING SEMICONDUCTOR HISTORY

Conducted a meticulous examination and characterization of seminal semiconductor devices including point-contact diodes, the pioneering Intel 4004 microprocessor, and the inaugural planar transistor (2N1613). Employed electrical characterization, SEM, and cross-sectional analysis to unravel their internal structures and operational principles. Deduced the process flows involved in their creation, and delved into the lesser-known historical narratives surrounding their development, shedding light on the early ingenuity that propelled the semiconductor industry.

#### SEMICONDUCTOR TRAINED AI

Developed a locally-run AI system trained on a comprehensive dataset of academic papers I've read and personal notebooks. This specialized AI serves as an interactive knowledge repository, assisting in generating ideas, answering complex semiconductor-related queries, and providing insights based on accumulated knowledge.